WHAT IS CLAIMED:

1. A phase-lock loop comprising:

an oscillator having an output oscillator signal whose frequency is related to a received error correction signal:

a phase-frequency detector receiving the oscillator signal and a reference signal and generating the error correction signal based on the phase difference of the oscillator signal and the reference signal;

a filter connecting the error correction signal from the phase-frequency detector to the oscillator, the filter including a capacitor;

a rate selector monitoring a charge on the capacitor and controlling the rate of error connection signals as a function of the charge on the capacitor.

2. The phase-lock loop according to Claim 1, wherein the rate selector sets the rate of the error connection signals to once per comparison cycle of the phase-frequency detector until the charge reaches a first threshold value and decreases the rate to less than once per comparison cycle after the charge has reached the first threshold value.

3. The phase-lock loop according to Claim 2, wherein the rate selector detects a plurality of increasing threshold values of charge and controls the variable rate to a corresponding plurality of decreasing rates.

4. The phase-lock loop according to Claim 2, wherein the rate selector includes a cycle counter to count the comparison cycles; and the rate selector uses the counter to set the variable rate.

5. The phase-lock loop according to Claim 2, wherein the rate selector sets a plurality of sequentially decreasing rates after the charge reaches the first threshold.

6. The phase-lock loop according to Claim 5, wherein the rate selector holds a minimum rate once the minimum rate is reached.

7. The phase-lock loop according to Claim 1, wherein the rate selector includes a counter to count the comparison cycles; and the rate selector uses the count of the counter and the capacitor voltage to set the variable rate.

8. The phase-lock loop according to Claim 7, wherein the rate selector controls uses the count of the counter to set a plurality of sequentially decreasing rates after the charge reaches a first threshold.

9. The phase-lock loop according to Claim 8, wherein the rate selector holds the rate at a minimum rate once the minimum rate is reached.

10. The phase-lock loop according to Claim 7, wherein the counter is a binary counter having more than L stages, where $1/(2^L)$ is the minimum rate; and the rate selector includes a logic circuit using the count of the stages and the voltage on the capacitor to set the rate.

11. The phase-lock loop according to Claim 10, wherein the counter has 2^L stages.

12. The phase-lock loop according to Claim 11, wherein the logic circuit sequentially decreases the rate to $1/(2^L)$.

13. The phase-lock loop according to Claim 12, wherein the rate selector holds the rate at the minimum rate once the minimum rate is reached.

14. The phase-lock loop according to Claim 10, wherein the logic circuit use the L and more than L stages until the rate reaches the minimum rate; and the logic circuit use the L stages to hold the rate at the minimum rate once the minimum rate is reached.

15. The phase-lock loop according to Claim 1, including a logic circuit between the phase-frequency detector and the filter which transmits the error correction signal through under the control of the rate selector.

16. A pulse width modulation controller including a phase-lock loop according to Claim 1; and wherein the reference signal is a master PWM signal and the oscillator signal is a slave PWM signal of the controller.

17. A power supply circuit comprising:

a main power supply;

a master PWM power supply that generates a first regulated supply voltage and a master PWM signal; and

a slave PWM power supply that receives the master PWM signal and generates a second regulated supply voltage and includes a phase-lock loop; and

wherein the phase-lock loop is according to Claim 1 and wherein the reference signal is the master PWM signal and the oscillator signal is a slave PWM signal used to regulate the second regulated supply voltage.

18. The power supply circuit according to Claim 17, wherein:

the master PWM power supply includes a soft-start circuit which generates a master disable signal during a predetermined master soft-start period beginning from start-up; and

the slave PWM power supply includes a soft-start circuit which disables outputting of the slave PWM signal for a predetermined slave soft-start period beginning from termination of the master disable signal, and the phase-lock loop operates prior to the termination of master disable signal to lock on the master PWM signal.

19. The power supply circuit according to Claim 18, wherein the master soft-start period is greater than a period of time for the slave's phase-lock loop to achieve lock.

20. A transmitter/receiver comprising:

a receiver circuit which generates a received base-band data signal from a modulated received signal and a local oscillator signal;

a transmitter circuit which generates a modulated transmission signal from a transmission base-band data signal and a local oscillator signal; and

a phase-lock loop coupled to the receiver and transmitter circuits; and

wherein the phase-lock loop is according to Claim 1.

21. A computer system comprising:

a central processing unit connected to a bus system;

a video processor connected to the bus system, controlled by the central processing unit and including a power supply circuit;

a display device connected to the video processor; and

wherein the power supply circuit is according to Claim 17.